ABSTRACT OF THE DISCLOSURE

A central processing unit (CPU) is described including a register file and an execution core coupled to the register file. The register file includes a standard register set and an extended register set. The standard register set includes multiple standard registers, and the extended register set include multiple extended registers. The execution core fetches and executes instructions, and receives a signal indicating an operating mode of the CPU. The execution core responds to an instruction by accessing at least one extended register if the signal indicates the CPU is operating in an extended register mode and the instruction includes a prefix portion including information needed to access the at least one extended register. The standard registers may be general purpose registers of a CPU architecture associated with the instruction. The number of extended registers may be greater than the number of general purpose registers defined by the CPU architecture. In this case, the additional register identification information in the prefix portion is needed to identify a selected one of the extended registers. A width of the extended registers may also be greater than a width of the standard registers. In this case, the prefix portion may also include an indication that the entire contents of the least one extended register is to be accessed. In this way, instruction operand sizes may selectively be increased when the CPU is operating in the extended register mode. A computer system including the CPU is also described.